

Proofing Tantalum Capacitors and Effects on Reliability

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Abstract

In traditional tantalum capacitors, the structure consists of a tantalum anode, the Ta₂O₅ dielectric, and MnO₂ as the initial cathode contact. The benefit of having MnO₂ in the cathode is the self-healing effect it provides. The conversion of MnO₂ to a higher resistive state (Mn₂O₃) allows the current within fault sites of the dielectric to be shut off from the rest of the capacitor. This self-healing phenomenon is a benign activity that leaves the capacitor functional to whatever voltage level is used to create this effect.

During the reflow solder process for surface mount tantalum chips, faults can be created or exacerbated to the point where the capacitor may fail at voltages below those previously experienced during the 100% electrical testing of these devices prior to packaging. To mitigate these faults developed during reflow, it is recommended for tantalum capacitors to be derated 50% for power-on reliability; but many times, customers are forced to use tantalum capacitors above the recommended range. To improve power-on reliability, we recommend proofing the capacitors. Proofing, or a controlled power up, is the process of activating the self-healing capabilities of tantalum capacitors. Although it has been shown to improve power-on performance and in some instances eliminate problems, the measurable effects of proofing have not been reported. This paper will reveal measurable effects of proofing.

Why is proofing required

The tantalum capacitor is typically built with three to four times the dielectric thickness required for its rated voltage. It is tested and exposed to voltages that are at least 132% of rated voltage, and it is usually used at applications voltages less than its rated. Then how is it that the dielectric can break down suddenly at voltages well below its rating?

The changes take place during the solder attachment process. This device is 100% electrically tested and put into pick-and-place feeder reels. In this position, the device still maintains the dielectric quality and capability verified through the electrical inspection. The pieces are removed from the reels, placed on the circuit boards, and then soldered, usually by reflow solder techniques. It is in this procedure that the device can change. Looking at the structure of the surface-mount tantalum capacitors reveals a metal pellet structure (tantalum, tantalum pentoxide, and manganese dioxide) surrounded by the plastic molding compound (Figure 1). The pellet is attached to the anode portion of the leadframe through a conductive epoxy that bonds two faces of the

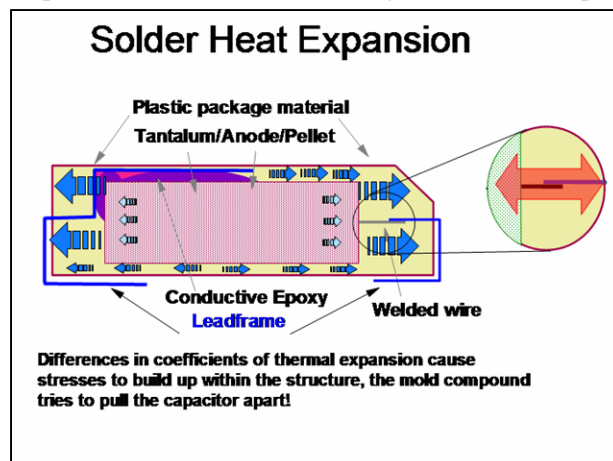


Figure 1. Mismatch of CTEs in tantalum solid-state capacitor.^[1]

pellet to the metal leadframe. The cathode riser wire at the other end of the pellet is welded to the leadframe at the opposite side to create the anode extension out of the plastic package.

During the solder operation, the entire package passes through the solder temperatures, causing the elements to expand at different rates according to each elements coefficient of thermal expansion (CTE). The plastic expands at a much greater rate than the metallic elements and this creates mechanical tensile forces on the pellet structure. This mismatch is made much worse once the temperature rises above the glass transition temperature of the plastic (approximately 180°C); where the expansion rate is close to double the initial rate for the duration that the device is held above this temperature. The longer the device resides at this temperature above the glass transition, the greater the magnitude of forces that the pellet must experience.

Looking at the structure in this state, the possible defects that might be created here are centered on the weld of the riser wire to the leadframe (anode) and the epoxy attachment of the pellet to the leadframe (cathode). Disruptions of these contacts could lead to high DF or ESR parameters in the capacitor, or an intermittent to open capacitance.^[1]

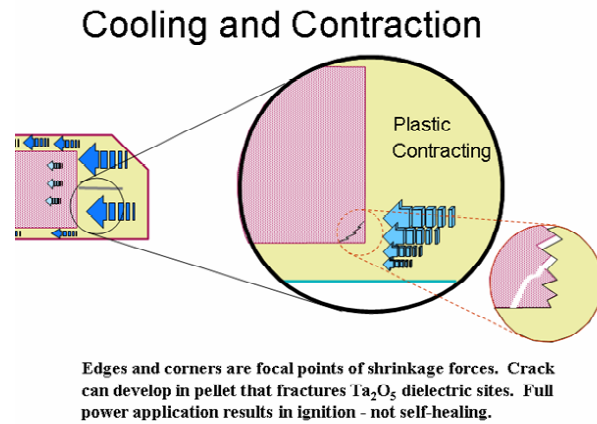


Figure 2. Contraction and compressive forces.

Once the device passes through the peak temperature of the reflow, the heat diminishes and the elements now begin to shrink, as they cool down. It is this aspect of the solder profile that we believe the damage is created to the dielectric that could lead to dielectric breakdowns. As depicted in Figure 2, the elements might not fit back together as perfectly as they once were before the heat generated expansion. Huge compressive forces could be placed on the pellet structure. Along the edges and corners, these forces could create a fracture in a very small portion of the pellet structure – if the pellet structure is fractured, there is a place in the dielectric where the dielectric is fractured.

Dielectric Fault Voltages

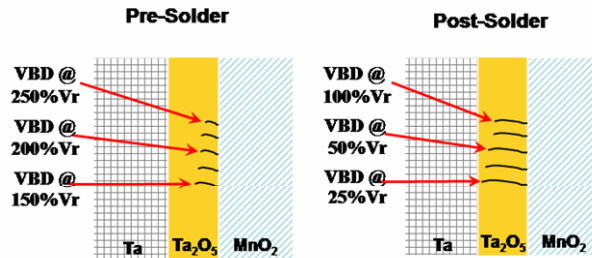


Figure 3. Fault expansion after solder process.

Even without the pellet fracturing, there may be enough compressive force on the pellet to allow a fault site in the dielectric that was not susceptible to voltages already experienced (132% of rated voltage), to grow or extend further into the dielectric to now become a breakdown site at voltages well below the rated voltage. This change in breakdown levels for the dielectric can be viewed in Figure 3. On the left are a series of faults as they might appear after 100% electrical testing and the pieces are placed in the reels. Though the faults exist, they are sensitive to voltages well above those of the rated and production test voltage. The diagram on the right might represent a post-solder condition where these faults have expanded further into the dielectric and now are sensitive to voltages at or below the rated voltage.

Though not shown, there are faults that exist in the pre-solder devices that are healed, whereby the MnO_2 has been converted locally at the point of contact with this material to Mn_2O_3 . This converted material has much higher resistivity and effectively pinches off the fault current into these points – eliminating them from the active capacitor circuit.

Proofing procedure

The devices tested were all similar devices (T491X226M035), from three different production batches. The samples were mounted on FR4 test cards using reflow profiles with peak temperatures around 232°C. Each test card held 20 pieces each, with a common terminal (anode) connected to one edge pin, and the 20 cathodes to individual pins along the card edge. “Proofing” involved the application of a selected DC voltage to each capacitor through a 1-kOhm resistor. After seven seconds application, the voltage across the capacitor was verified to be within 99% of the applied voltage. If the voltage was less than this level, the capacitor was charged for another seven seconds and the level was again verified to be within 99% of the applied voltage. If the voltage is still below 99% of applied after second seven-second interval, the piece is rejected.

Out of each batch, a control group was created to see the effects of “no proofing,” and three additional groups of “proofed” capacitors were created at rated voltage (35 VDC), rated voltage plus one VDC (36 VDC), and rated voltage plus four VDC (39 VDC). The three batches tested were pulled from production lots where two of these batches (BN10 and HK40) were rejected because of unacceptable losses during electrical testing (and HJ40 is the ‘good’ batch). There were three pieces rejected for failing to meet the 99% applied voltage between the two ‘bad’ groups.

I. Scintillation Test Results

Scintillation testing consists of the application of a small constant current to each capacitor and monitoring the voltage rise versus time.^[2] The theory is that the voltage will continue to rise until the voltage reaches a predetermined compliance level or until the weakest dielectric point is achieved (the scintillation or breakdown voltage for that piece). Secondary scintillations may be at different points within the dielectric (these should

always be at higher level than any previous), but may also be the result of consequential cracks or secondary fault sites created by the energy burst of the initial scintillation (allowing secondary scintillations to be of lower magnitude than any previous). The initial scintillation voltages from a group of pieces then represent a cumulative indication of the dielectric quality (fault distribution) for that group.

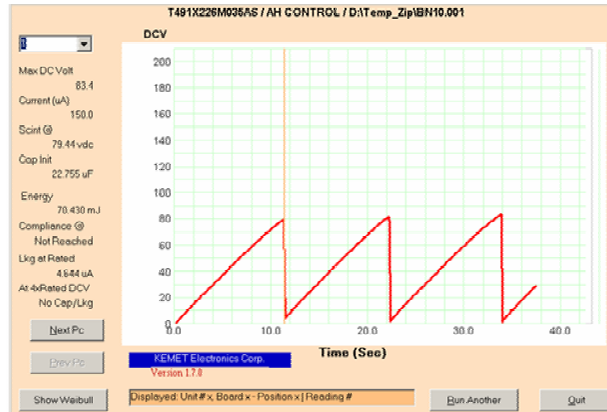


Figure 4. Scintillation event for single piece.

The scintillation test for one of the pieces is captured in Figure 4. The constant current was selected to be 150 uA, and there is an initial dv/dt that rises up to 79.44 VDC, and then collapses down below 5 VDC. The difference in energy levels represents a change in energy of 70.43 mjoules. The scintillation test is run at room ambient temperature.

We also use the dv/dt of the 1st eight points to estimate the capacitance (assuming no leakage current at these very low voltages), shown here as 22.755 uF. Once we establish the capacitance, we then assume that a change in the dv/dt slope for the 5 points nearest the rated voltage are due to the loss of charging current as leakage current, and an estimate of the leakage current is shown to be 4.644 uA. The scintillation voltage ranking for each piece represents the first scintillation voltage level, or as in the case of this piece at 79.44 VDC.

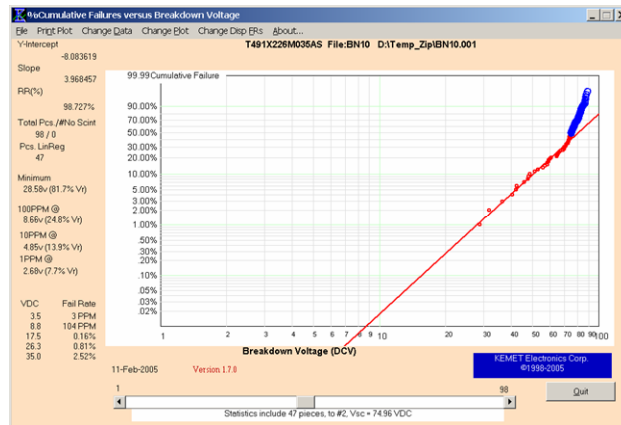


Figure 5. Weibull plot of data with linear fit.

Figure 5 represents the collective scintillation voltages for a single group of 98 pieces, with the cumulative percentage (Y-Axis) plotted against the scintillation voltage level (Breakdown Voltage or X-Axis). A linear fit is established for the lower voltages through 47 of the 98 points. The points selected are those that give the best correlation coefficient (RR). Projecting the linear fit allows a projection of the voltages required to

achieve 1, 10, and 100-PPM failure rates although the confidence bands (not shown) get wider as the linear fit moves away from the data population or the mean.

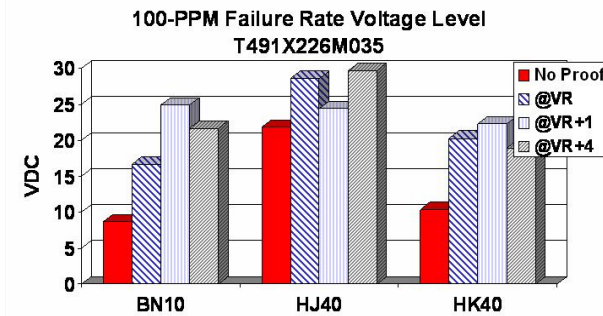


Figure 6. Scintillation projection of 100-PPM FR voltages.

The results of this testing on the three batches and their four subgroups of capacitors results in the 100 PPM failure rate (FR) voltage levels as shown in Figure 6. The three batches are identified as BN10, HJ40, and HK40. The leftmost bar in each batch represents the control group, or pieces that were mounted and tested, with no proofing. In order from left to right in each batch, are the groups proofed at rated voltage (V_R), V_R+1 VDC, and V_R+4 VDC.

The BN10 and HK40 ('bad') groups show a large variation between the control groups and the proofed groups, whereas the HJ40 ('good') batch does not show this variation. One would think that as the proof voltage is increased, there would be a direct correlation between that magnitude and the 100-PPM failure rate levels, but this is not the case. These voltages are not that much different, and the reduced level of confidence at the 100-PPM extrapolation may have a bearing on this blend.

Looking at a failure rate of a voltage level closer to that of the data collected would allow a tighter confidence. In Figure 7, the failure rate at the recommended application voltage of $\frac{1}{2}$ of V_R reveals a much more extreme separation between the control (no proofing) and all the proofed groups for the two 'bad' batches. It is also apparent that the 'good' batch, HJ40, was not affected as much as the other two. This brings up one of the reasons why some batches appear to cause problems, and others do not. Proofing HJ40 had no considerable impact on the failure rate at 50% V_R , whereas there were large impacts on batches BN10 and HK40.

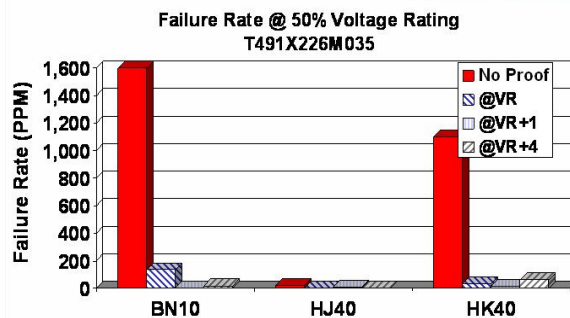


Figure 7. Scintillation projected failure rates at 50% V_R .

II. SSST Test Results

In a nearly opposite approach to scintillation testing, SSST (Step Stress Surge Test ^[3]) evaluations use as large of a current as possible to drive the voltage across the capacitor to a predetermined level, as quickly as possible. A high power, high current source is supplemented with a large bank of capacitors across the output of the

supply to allow as quick a transfer of energy as possible. The energy is switched through three parallel FETs, each with an $R_{DS_{ON}}$ resistance of 10 milliohms.

The testing normally starts at 50% of V_R , and is incremented only after the capacitor withstands four ‘ON’ pulses and four ‘OFF’ pulses (duration is $\frac{1}{2}$ second ‘ON’ and $\frac{1}{2}$ second ‘OFF’) for that voltage level. In a 10-millisecond window before the pulse is transitions to ‘OFF’, the voltage across the test capacitor is measured and must be within 90% of the applied voltage to be considered successful. Falling below this level indicates a failure. The purpose of this test is to mimic a power-on condition of unimpeded current, and to drive the fault to a catastrophic failure.

In the same manner as scintillation testing, the breakdown voltages for a group of pieces are analyzed to create a linear fit and allow an extrapolation of the low PPM failure levels. As with the scintillation test, the center group of Figure 8, HJ40, appears to be least effected by the proofing, as the difference from control to the proofed groups seems minor.

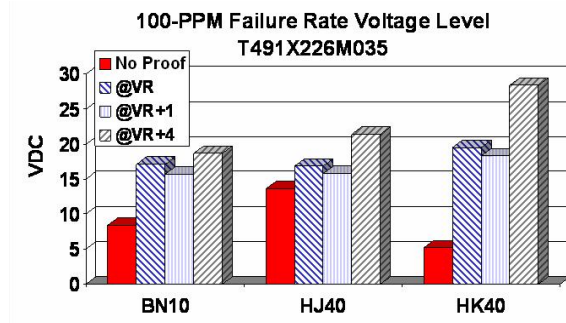


Figure 8. SSST projections of 100-PPM FR voltages.

As with the scintillation data, the differences of the different proofing voltages appear inconsistent when comparing the 100-PPM levels. Again, because of the wider confidence spread for this extrapolated level, using a level closer to the distribution of the data points will reduce the confidence range and uncertainty. Looking at that data as the failure rate at 50% of V_R as in Figure 9, the plot is very close to that of the scintillation test of Figure 7.

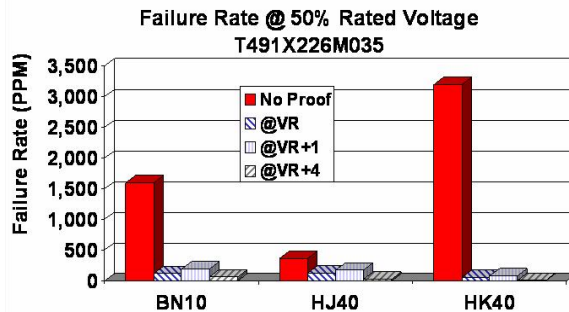


Figure 9. SSST derived failure rates at 50% V_R .

The control group (No Proof) of batch HJ40 shows relatively low initial failure rates at the 50% V_R level – nearly equal to those failure rate levels achieved with the other two batches, BN10 and HK40, after proofing. This reinforces the concept that there is difference in these batches after the solder process, with batches BN10 and HK40 being weaker.

III. Life Test

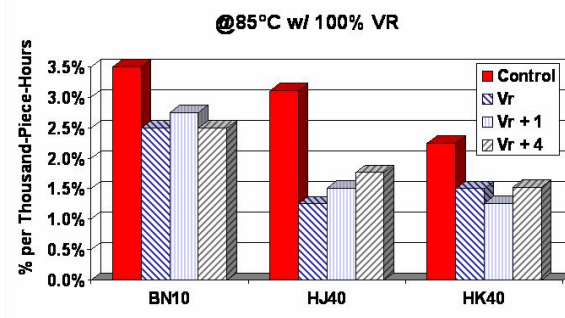


Figure 10. Life test results – failure rates per thousand-piece-hours.

The SSST and scintillation test were devised to show initial power-on failures or those associated with a sudden increase in the applied voltage. The results in this life test were intended to show the effects of proofing on the failure rate for long-term reliability. The pieces were stressed with 100% of rated voltage at a temperature of 85°C for 2,000 hours. The plot in Figure 10 shows this comparison for each batch compared to the control of that group. In this comparison, there is a large separation between the control group and the proofed groups, though there is no consistent correlation between the failure rates and the level of the proofing voltage. This comparison is highlighted in Figure 11 which compares the changes in failure rates referenced back to the failure rate of the control for each batch.

Again, there is a clear improvement in failure rates once any proofing is accomplished, but there is no correlation to the level of the proofing voltage.

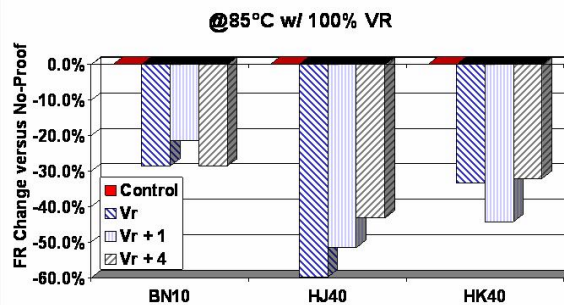


Figure 11. Changes in life test failure rates referenced to control for each test batch.

Conclusions

The effects of the proofing are in line with the supposition that clearing the dielectric of these fault sites enhances reliability of the component, but most significantly in weaker components. Variations from batch to batch could present groups where this procedure has little effect, but it will have effect on the weaker batches to bring them up to the capability of the stronger batches. Variations in solder may create these same good/bad variations. With the higher peak temperatures and durations above 180°C increasing for Pb-Free solders, so will the likelihood of failures increase. As the application voltage (with respect to the rated voltage) increases, the more likely that proofing will impact the failure results.

These test shows similar effects in proofing when comparing short-term tests (scintillation and SSST) and long-term testing (life test). There is a substantial increase in reliability from the ‘no proof’ to the ‘proofed’ groups, but there is no correlation among the various proofing voltage levels and the failure rates.

Testing with substantially larger samples of 1,000 pieces or with larger separations of the proofing voltages may allow for a response that is proportional to the magnitude of the proofing voltage, but once we committed to using these pieces from those “bad” batches, we were limited to the pieces remaining as other investigative tests depleted the pieces remaining. It may also be advantageous if the piece type selected were not of a ‘troublesome’ nature.

In almost every case where power-on failures presented a problem to a specific customer, or a specific circuit assembly, we have been successful in greatly reducing or eliminating these failures. Only with instances where the failure rates were huge to begin with, were we unable to bring that down into an acceptable range. If the batch is poor to begin with, then the solder activation of fault sites may be a minor contributor to the overall poor performance.

Bibliography

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