

Embedded Passive Components to Increase the Reliability of High Frequency Electronic Circuits

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Abstract

Usually, the majority of passive devices employed in electronic systems are discrete components. Small discrete devices dominate the area of PCB mounted process in a typical electronic product. For example, a cellular phone may consist of only about 20 integrated circuits (IC) compared to 300-400 passive devices. Thus, passive components have substantial influence on system cost, size, and particularly reliability. In order to meet the next generation electronic packaging requirements (smaller, faster, cheaper, and more reliable), alternatives to discrete passives are necessary. In this paper we present a help to design embedded capacitor for high reliability applications.

Introduction

Passive devices represent a significant number of components to be reflow on a PCB. The use of discrete passive components in electronic systems has continued to increase as the degree of system integration has increased. While many people thought that discrete passives would be “integrated” away into integrated circuits, exactly the opposite has happened. In 1984, passive devices represented 25% of all components on printed wiring boards; by 1998 this fraction grew to over 90%, [1]. The demand for faster clock speeds, lower operating voltages, higher IO counts, and combined analogue and digital functionality have all contributed to an higher demand for passive devices.

Moreover, passive components manufacturer regularly follow the technological development of the active components by increasing their energy storage capacity and reducing the volume of the device. Passive devices become very difficult to assembly on a traditional printed circuit board. The size reduction between patterns induces crosstalk risk. So manufacturers wish to establish the passive either directly in the substrate [1] or to integrate them in dedicated silicon chips [2]. All these innovations are also related to the interest of SiP (system in package) to the detriment of the SOC (System on chip).

This last technology is very limited by two problems: the Time To Market which becomes increasingly short and the competition between manufacturers of active components who disperses the areas of supply active chips around the world for a given electronic function. Finally, two parallel phenomenons are present: the need of high frequency applications and the scale reducing of the devices. Now a new constraint happened, the scale of the pattern is identical to the wavelength of the signal. This evolution of the electronic circuit for high frequency applications is summarised on the figure 1.

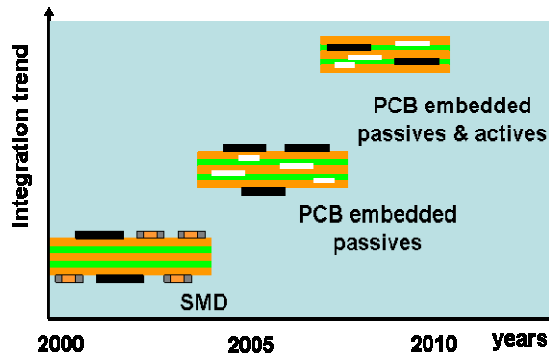


Figure 1: Integration trend vs years – evolution for the package in the future

The potential advantages to integrate passive components in the PCB for many applications are related below:

- Increase circuit density through saving real-estate on the substrate
- Decrease product weight
- Improve electrical properties through additional termination and filtering opportunities and shortening electrical connections
- Cost reduction through increasing manufacturing automation
- Increase product quality through the elimination of incorrectly attached devices
- Improve reliability through the elimination of solder joints.
- Increase the difficulties to operate a “reverse engineering”

In this paper, we show a method of design for embedded capacitors in a PCB and we will apply this rule to three examples. We will discuss then on the tools necessary to analyse this type of components and we will evaluate the difficulty which lies in the analysis of the reliability of a PCB which is none a distinct component and not only a mechanical medium.

Design rules for embedded capacitors

In the framework of a European project, we are working to the development of a low cost technology binding for high frequency circuits with digital circuits of treatment of data and measurement. Decoupling becomes one of the most important needs to integrate the capacitors in printing wired board. The guideline for decoupling high speed circuits is to mount capacitor as close to the IC. One strategy is to place the capacitor directly in the board under the circuit. In the present study, dedicated to the embedded capacitors; we also consider an alternative solution using the frame of the package. Embedded capacitor is one possible solution for integral capacitor if the dielectric constant and the thickness of the layer are well controlled.

Dielectric constant

For thick film technologies as hybrid or PCB specific dielectrics [3] exist. Dielectric constant values about 10 to 50 for typical thickness from 3 μ m to 100 μ m are common. The surface of the future capacitor is an important parameter to study. The most pertinent characteristic to study is the variation of the real part of the permittivity of the

dielectric versus the surface of the capacitor. So it is useful to study the variation of the surface of the capacitor versus the real part of the permittivity of dielectric used (see figure 2).

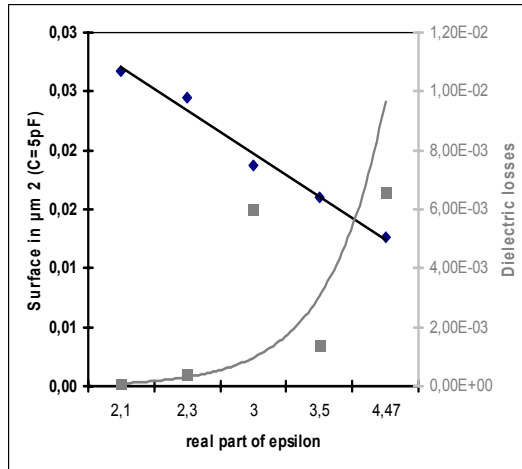


Figure 2: Variation of the surface and the dielectric losses vs real part of permittivity

In fact the value of the surface decreases with the increase of the value of the permittivity. Generally the dielectric losses in polyimide materials are not enough low for RF applications. For example the losses in a polyimide substrate become too strong at 5 GHz. This point has to be improved for the latest application. Interconnections are also important to be study [4] as well as the thickness of the dielectric.

Modelling of embedded capacitors

First the capacitive structure can be studied through an simple equivalent electrical circuit presented figure 3, where C represents the capacitor, C_p and L_s the intrinsic parasitic elements of the structure and L_m the connection elements.

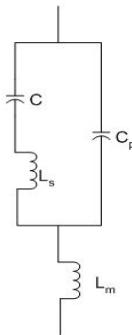


Figure 3: Electrical model

In this model [5, 6], the equivalent impedance Z_{eq} can be written as :

$$Z_{eq}(p) = \frac{1 + [L_s \cdot C + L_m \cdot (C + C_p)] \cdot p^2 + L_m \cdot L_s \cdot C \cdot C_p \cdot p^4}{(C + C_p) \cdot p \cdot \left[1 + L_s \cdot \frac{C \cdot C_p}{C + C_p} \cdot p^2 \right]} \quad (1)$$

Noting C_0 is the low frequency value of C_{eq} , ω_1 and ω_3 the poles and ω_2 the zero of Z_{eq} , the following relations are obtained for C , C_p , L_s et L_m :

$$C = - \frac{(\omega_{1^2} \cdot \omega_{3^2} - \omega_{2^2} \cdot \omega_{3^2} - \omega_{1^2} \cdot \omega_{2^2} + \omega_{2^4}) \cdot C_0}{(\omega_{1^2} - \omega_{2^2} + \omega_{3^2}) \cdot \omega_{2^2}} \quad (2)$$

$$C_p = \frac{\omega_{1^2} \cdot \omega_{3^2} \cdot C_0}{(\omega_{1^2} - \omega_{2^2} + \omega_{3^2}) \cdot \omega_{2^2}} \quad (3)$$

$$L_s = - \frac{(\omega_{1^2} - \omega_{2^2} + \omega_{3^2})^2 \cdot \omega_{2^2}}{(\omega_{1^2} \cdot \omega_{3^2} - \omega_{2^2} \cdot \omega_{3^2} - \omega_{1^2} \cdot \omega_{2^2} + \omega_{2^4}) \cdot C_0 \cdot \omega_{1^2} \cdot \omega_{3^2}} \quad (4)$$

and
$$L_m = \frac{\omega_{2^2}}{C_0 \cdot \omega_{1^2} \cdot \omega_{3^2}} \quad (5)$$

For the different applications and structures that are considered, these parameters will be extracted from the frequency responses of the embedded pattern. We will try to link these parameters to the reliability of the capacitor.

Frequency behaviour and design

Two type of structure were designed: one layer and multilayer. The monitoring of the frequency response will allow us to choose the best configuration.

a) One layer structure: For planar structure, the value of the capacitance is given by the following formula:

$$C = \frac{\epsilon_0 \cdot \epsilon_r \cdot S}{h} \quad (6)$$

where ϵ_0 , ϵ_r are respectively the primary electric constant and the relative permittivity of the material, h is the thickness of the dielectric and S the surface of the electrodes.

For high frequency applications, the frequency response of the capacitor (resonance frequency) is related to the size of electrode which is equal to a quarter wavelengths. By this way, for a given capacitor value and a wished operating frequency f , the best compromise is obtained by squared electrodes with lower or equal dimension to a quarter of the wavelength at the chosen frequency.

In previous relations, the value of the electrode surface is replaced by a square one with a

$\lambda/4$ size, and we obtain a surface about $\lambda^2/16$. Recording that λ is given by $\frac{c}{\sqrt{\epsilon_r} \cdot f}$

where c is the velocity of light in vacuum ($3 \cdot 10^8$ m/s) and f the used frequency, the surface of the electrodes becomes

$$S = \frac{c^2}{16 \cdot \epsilon_r \cdot f^2} \quad (7)$$

Including (7) in (6) the expression of C becomes:

$$C = \frac{\epsilon_0 \cdot c^2}{16 \cdot h \cdot f^2} \quad (8)$$

The first observation of the relation (8) shows, C is now independent of the dielectric constant (ϵ_r). It is also interesting to formulate the equation (8) under the following format:

$$C \cdot f^2 = \frac{\epsilon_0 \cdot c^2}{16 \cdot h} \quad (9)$$

Finally we can note that for a wished capacitor value and a given technology (h fixed), this relation gives the frequency range that could be obtained.

b) Multi layer structure: For a multilayer structure, we have to consider

- the additive law of capacitance value versus n the number of layer:

$$C = n \cdot \epsilon_0 \cdot \epsilon_r \cdot \frac{S}{h} \quad (10)$$

- the law that gives the first resonance frequency versus the number of layers:

$$f_1 |_{nlayer} = \frac{f_1 |_{layer}}{\sqrt{n}} \quad (11)$$

We can define also a simple relation as written in the relation (9).

c) Design rule: In conclusion, for a squared electrode structure (either simple or multi layer) and a given technology related to the layer thickness h, the best compromise between the capacitor value C and the maximum operating frequency range f is given by :

$$C \cdot f^2 \leq \frac{\epsilon_0 \cdot c^2}{16 \cdot h} \quad (12)$$

This result is very interesting for design rules of embedded capacitors.

We have performed a Design Of Experiment (DOE) method to optimise the wavelength versus frequency (see figure 4) and ϵ_r between 10GHz to 20GHz.

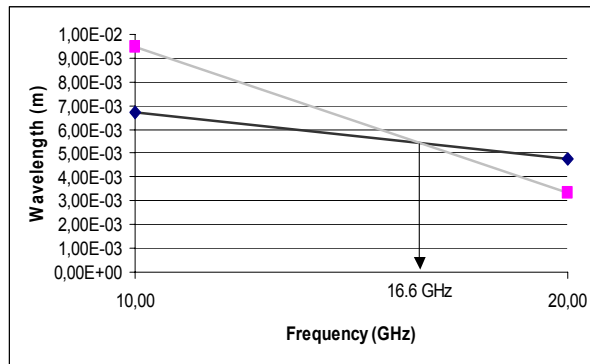


Figure 4: DOE result for wavelength determination

The results give an optimised value at 16.6GHz for $\epsilon_r=15.6$. Figure 5 proposes the variation of the capacitance versus the thickness of the dielectric. The importance of the dielectric thickness is well shown.

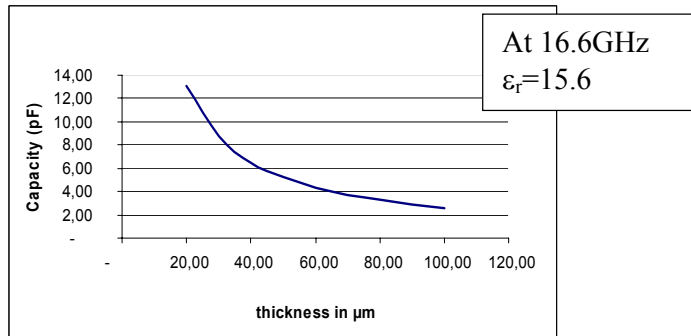


Figure 5: Variation of the capacitance versus dielectric thickness for an optimised wavelength point

Applications

Two applications will be presented in the next paragraph. Those applications are linked to the ceramics material used in LTCC (Low Temperature cofired Ceramics) capacitors for the first example and for the second one a polymer dielectric from ROGERS and used for MCM-L (Multi Chip modules Laminated) applications is considered.

Ceramics capacitor

First application concerns the ceramics capacitors. Some techniques are used to embed ceramics capacitors in various types of substrates [5]. The thickness of the component is reduced to correspond to the substrate size by a mechanical polishing. In order to verify previous relations (7), (8), (9) and (12), such capacitors have been studied.

The MLCC manufacturing gives two following data: $C = 22\text{nF}$ and $\epsilon_r = 2100$. Then we have made a DPA (destructive physical analysis) to evaluate the technological parameters of this multilayer component (size of the electrodes and the dielectric thickness), see figure 6.

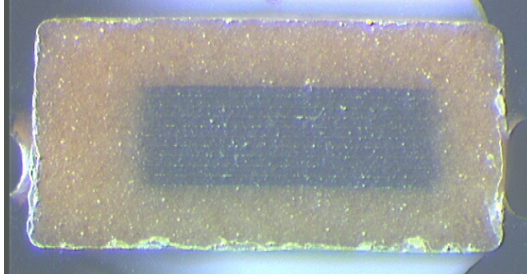


Figure 6: Micrograph of a ceramic capacitor (magnification x50)

The DPA shows an average thickness of the dielectric layer about $25.2 \mu\text{m}$ and the electrode dimensions are: $1334.02 \mu\text{m} \times 767.91 \mu\text{m}$ and there are 26 layers. With those parameters it is possible to calculate the capacitance of this capacitor and to determine the cut off frequency of this device. So applying (10), C is equal to 19.7nF and by (12) f is found at 317 MHz .

Due to the inductive effect of the interconnections and the form factor of this structure (rectangular one) we measured a lower value for the frequency close to 200MHz . This result is in good agreement with the theoretical approach.

Other ceramic capacitor used in high frequency application was studied (DICAP 43pF one layer). The DPA analysis is presented on figure 7.

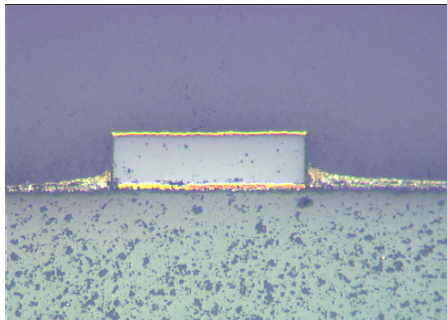


Figure 7: One layer ceramic capacitor (magnification x10)

With the formula (12) we found a maximum operating frequency value of 3.4 GHz . Measurement done with HP network analyser (8720D) gives a lower value ($<1\text{GHz}$). This is due to the interconnection set.

ROGERS materials

In the second application, we study the realization of embedded capacitive structure within the multi-layer frame of the package [7, 8]. Two different dielectric materials are considered for these structures. They are Rogers's products with the following characteristics:

R1: thickness: $e = 50\mu\text{m}$; Dielectric constant $\epsilon' = 10.73$; Losses : $\tan \delta = 0.0029$

R2: thickness: $e = 100\mu\text{m}$; Dielectric constant: $\epsilon' = 12.8$; Losses : $\tan \delta = 0.0034$

With R1 material

Various structures were considered in simple layer, 4 layers and 8 layers respectively referenced C1, C4 and C8. They are first of all simulated using the software 3D finite elements HFSS, then carried out and measured with a HP network analyser. For a chosen frequency range we can extract the parameters of the model with the according equations (2), (3), (4) and (5) the respective values from the elements of the model are extracted. Table 1 summarizes the measurement results.

CAPA	Measurements				Extracted values			
	C0 (pF)	f1 (GHz)	f2 (GHz)	f3 (GHz)	C (pF)	Cp (pF)	Ls (nH)	Ln (nH)
C1	5.46	1.32	4.47	9.14	4.85	0.61	2.35	0.64
C4	22.69	0.59	3.96	6.88	21.94	0.74	2.25	1.06
C8	47.82	0.392	3.24	3.47	42.90	4.92	0.55	3.00

Table 1: Measurement results and extracted values – R1 material

The obtained values of the capacitors are coherent with the required ones. The obtained value of the capacitor varies with the number of layers according to the relation (11) (figure 8).

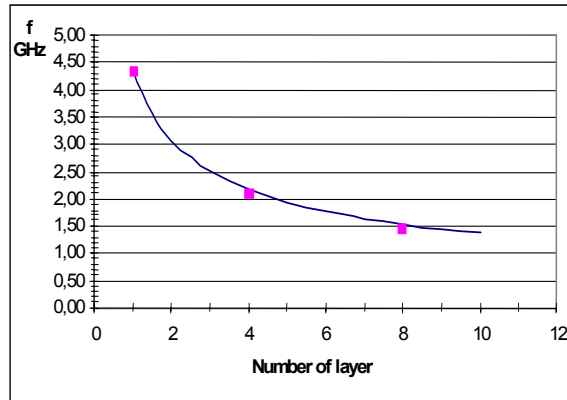


Figure 8: resonance frequency law versus number of layers

However the parasitic parameter in the case of multilayer device worsens the frequency performance. The interdigitated structure contains several inductive patterns. This pattern added degrades the maximum working frequency. The geometry of the structure and the interconnections are critical elements which must be improved.

With R2 material

With this material, a working frequency up to 10GHz requires squared electrodes with side dimension equal to $w = 2\text{mm}$, and the value C is about 5 pF for one layer structure. In order to obtain a 15pF capacitor, we have considered a three layers structure. According to the relation (12), the maximum operating frequency is found at 5.75GHz.

These structures are simulated considering different length for the access line and the results are presented in the following table 2.

Access line length	Simulated results				Extracted values			
	C0 (pF)	f1 (GHz)	f2 (GHz)	f3 (GHz)	C (pF)	Cp (pF)	Ls (nH)	Lm (nH)
l ₁ =1mm	14.7	1.98	7.34	7.76	8.42	6.25	0.13	0.40
l ₂ =3mm	14.9	1.35	7.14	7.42	9.85	5.03	0.15	0.86
l ₃ =39mm	19.7	0.394	1.33	2.47	17.35	2.36	6.94	2.39

Table 2: Simulated results and extracted values – R2 material

The table 3 gives shows the measurement results for two samples and the extracted values.

CAPA	Measurements				Extracted values			
	C0 (pF)	f1 (GHz)	f2 (GHz)	f3 (GHz)	C (pF)	Cp (pF)	Ls (nH)	Lm (nH)
Ca	15.8	0.65	3.36	6.55	15.06	0.79	2.97	1.00
Cb	16.7	0.64	3.25	6.40	15.86	0.86	2.93	0.96

Table 3: Measurement results and extracted values – R2 material

Considering all the connecting elements brought by test fixture (SMA connectors) as an access line of about 5mm length, the measurement results present a good agreement with the simulation and the frequency behaviour is in accordance with the theoretical law (12).

Discussion

We have shown that all the technologies dedicated for the embedded capacitors are very interesting. They are all made for two main goals: first to reduce the size of the component and to reduce also the risk during the mounting process and secondly to reduce the cost of the final circuit. Moreover the increasing of the dielectric's constant value induced an increase of the losses and this result does not still lead with the high frequency applications.

Components analysis

The technologies available for the packaging of microelectronics at that time were generally thick film and thin film circuits [9, 10] hermetically sealed in a package made of ceramic or metal with glass to metal feed-through. The need for a package, to interconnect board plus discrete passives components complicates the assembly of the hybrid microcircuit and increases volume and weight requirement. It is why an important number of manufacturers are working on new based polymer materials compatibles with the PCB substrate [11, 12]. The difficulty is to characterize such components embedded in the PCB or the hybrid. One solution resides in the use of isolation current and dielectric losses measurement.

So embedded capacitors seems promote to a very interesting future [13, 14, 15]. But, for this kind of technologies: How to extract information about reliability?

Predictive reliability during conception

Conventional methods of analyses such as acoustic microscopy or the X-ray are not adapted to the printed circuits containing FR4. Acoustic waves cross with difficulty PCB fibres (due to the length width) and the X-ray do not detect delaminations or cracks.

For such technologies it is necessary to study reliability during the design of the product: size of the component, number of capacitors to be embedded, positioning in the substrate...

Engelmaier and Clech shown in their articles [16, 17] that strains in solder after the assembly process of a capacitor are about 300MPa for a traditional reflow process on PCB. Today electronic devices, which are used in all human activities, have to support harsh conditions of use especially in automotive industries. That extremely severe mission profiles are also associated to a rising complexity of electronic components technology, which makes parts more sensitive to a large panel of constraints. This situation needs a complete renewal of the reliability approach. The reliability must now be evaluated since the design process. This predictive approach needs a specific database with material and methods regularly changed and upgraded. This database EURELNET (European Reliability Network) [18, 19] exists since 2002. In the framework of EURELNET we developed specific tools to help designer in order to integrate reliability during the product design. CRITIDEL is one of those program and we have study with this program, just after the laminate process, the strains at the interfaces (see figure 9) between the copper layer and the PCB and the interface between the copper layer and the dielectric material. For the calculus we have used the following values: PCB CTE of the FR4 close to 16, the CTE value of the polyimide 25 and the length of the square embedded capacitor 30 mm.

Figure 9 shows that the strain value on the top and the bottom of the dielectric is less than the value calculated for a capacitor reflowed on a PCB (close to 8MPa to 10MPa instead of 300MPa). The second interest of this model is the possibility to reach a thickness value which is strain less: 12 μ m.

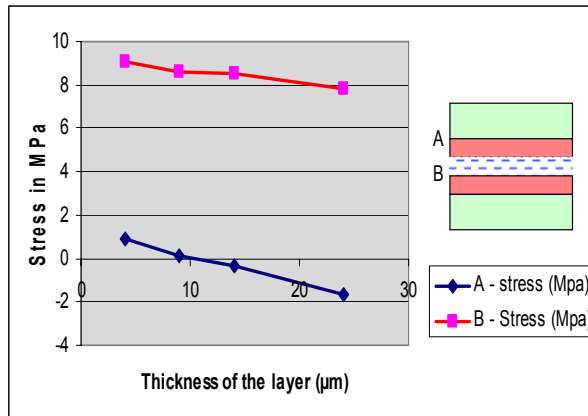


Figure 9: Strain value in the copper-dielectric and copper-PCB vs thickness of the dielectric for the capacitor calculated with CRITIDEL.

Conclusion

However, the need of a high capacitance at a high frequency is difficult to obtain. In the different studied applications, the formula (12) is validated. It demonstrates that the

dielectric constant is not really the principal parameter and the thickness plays a more important role. It is shown that this result is independent of the number of layer and so it can be considered as a good rule for the designer in order to determine the maximum possible capacitance value at a fixed frequency and chosen technology (dielectric thickness).

Characterizations of embedded capacitors seem very difficult to proceed but electrical analysis would be able to notify if the process is well done. Embedded passives are more reliable by eliminating solder joints; they also introduce other potential defects such as cracks, material mismatch, delamination, etc. But we have seen that the strains at the different interfaces are less than a solder joint, it is a good result for the reliability point of view. In the framework of the European programme HIFAP we will studies new materials for embedded capacitors and their reliability during their profiles mission.

Acknowledgements

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