

# Addressing Tantalum Capacitor Technology Challenges

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## ABSTRACT

Providing highest capacitance possible in small package remains the major challenge for Tantalum capacitors industry. This means providing customers with the highest capacitance possible while saving product board space. The volumetric efficiency of capacitors made by traditional leadframe technology decreases as case sizes becomes smaller. Thus, improving package volume utilization in small case sizes is particularly important. The best solution is to create lead frameless construction as well as to minimize the wall thickness of plastic the encapsulant.

This paper will describe a new packaging technology that enables a twofold increase in volumetric efficiency in 1608-case-size molded chip tantalum capacitors. Process concept, performance characteristics, and product range will be presented.

## INTRODUCTION

The ongoing trend of miniaturization requires increasingly smaller components.

Delivering the best volumetric efficiency has always been the strongest advantage of solid tantalum capacitors. As is well known, this volumetric efficiency is the result of efficient utilization of package volume combined with usage of high charge tantalum powders. Component miniaturization and reduction of the component profile have become important as well.

Most of new consumer devices are small and thin, and thus requiring low-profile components.

Suitable capacitor types include MLCC and tantalum. In recent years, MLCC technology has advanced into the high capacitance area, and now competes with tantalum technology in the 1608, 2012, and 3216 case sizes.

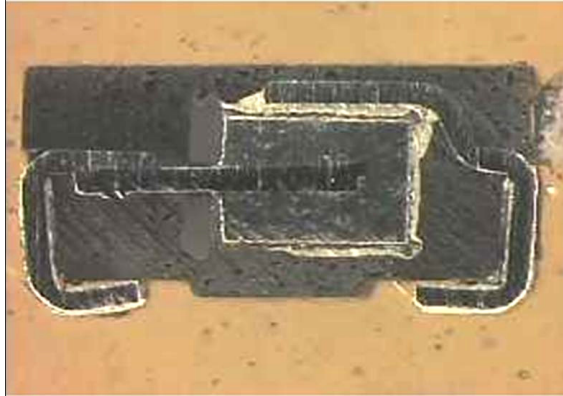
For example, in the 1608 size both technologies offer a 10 $\mu$ F capacitance value. However, the best possible 10 $\mu$ F–6V tantalum capacitor in leadframe construction does not present any significant advantage over a 10 $\mu$ F–6V MLCC.

A new approach is needed in order to provide tantalum capacitors with significantly higher capacitance values. This paper will describe novel methods of capacitor assembly,

encapsulation, and termination that enable a twofold increase in volumetric efficiency in 1608-case-size molded chip tantalum capacitors.

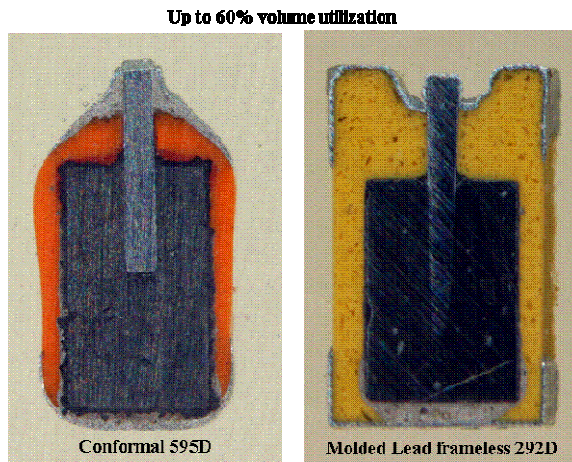
### **MINIATURIZATION IN TANTALUM CAPACITOR PACKAGING TECHNOLOGY**

The traditional packaging technology for molded tantalum chips is well established. Capacitors as small as the 1608 footprint, usually referred as J case, have been created as part of the ongoing quest for miniaturization. However, leadframe technology is quite limited in its volumetric efficiency (Fig 1), so such capacitors cannot sufficiently compete with other dielectrics.



**Fig.1. Traditional molded tantalum chip construction.**

Vishay presently uses two advanced techniques for improved volumetric efficiency. Representative products are conformal-coated chips (592D, 595D, 572D, etc.) and leadframeless 292D chips (Fig 2). Both families offer excellent products in the 2012 package size.



**Fig. 2. Conformal-coated chips (592D, 595D, 572D, etc.) and leadframeless 292D chips.**

However, the 2012 case size is probably the smallest possible with conformal-coated packaging technology: at smaller sizes, proper control of rectangular unit shape becomes too difficult to achieve and thus is not economically feasible.

Producing leadframeless 292D chips in the 1608 case size via the conventional tantalum technology of transfer cavity molding has been found to be not economically feasible.

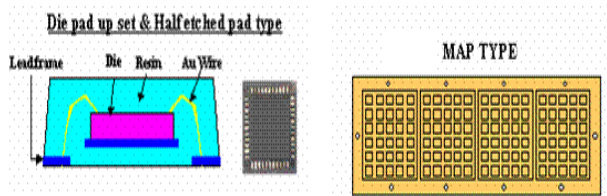
Therefore, a new approach was required to develop a high performance tantalum chip that could become a product of the future.

This new product should have the following features:

1. highest volumetric efficiency to maintain a competitive edge against MLCCs
2. capability of further downsizing to 1005 case size
3. molded package with well defined dimensions and terminations for easy pick up and board mounting.

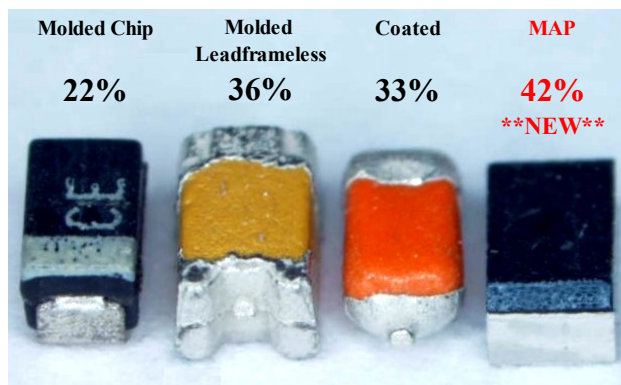
Multi-array packaging (MAP) technology, which in fact has been used to produce many semiconductor devices in QFN (quad, flat-pack, no-lead) style packaging, was found to be the most appropriate technology for the new Tantalum capacitor.

The general idea of MAP technology is to create an array of components that is efficiently handled as a group and is cingulated only during final operations. Fig. 3 shows a cross-sectional view, final product, and leadframe for typical QFN devices.



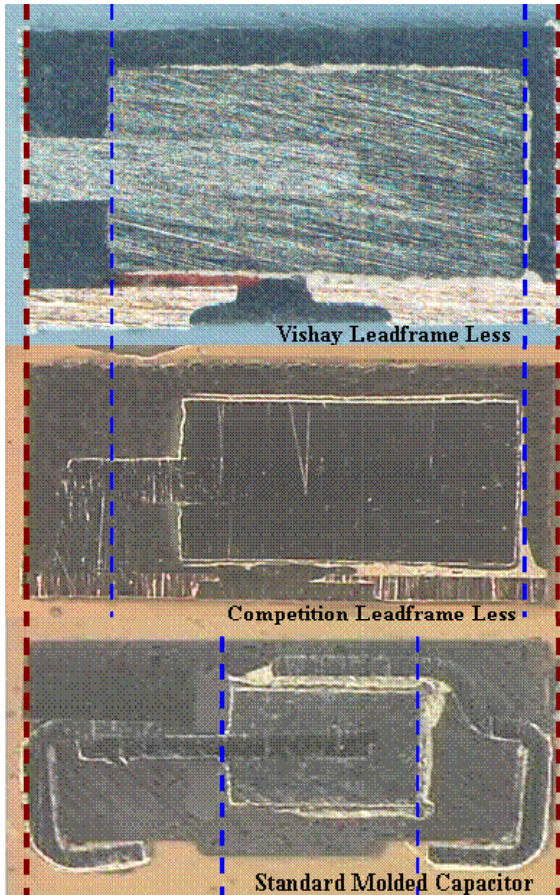
**Fig. 3. QFN Cross-sectional view, final product, and leadframe.**

The MAP platform combined with a state-of-the-art, patented<sup>1,2</sup> Vishay termination process results in a new 298D consumer product with extremely high volumetric efficiency (Fig. 4) as well as in TM8 High Reliability product series.



**Fig. 4. Volumetric efficiency of various packages in the 2012 P-case.**

Several tantalum capacitor manufacturers offer advanced products with “leadframe-less” designs. The Vishay 298D has a distinct volumetric advantage due to external connection between the anode wire and termination (Fig. 5).



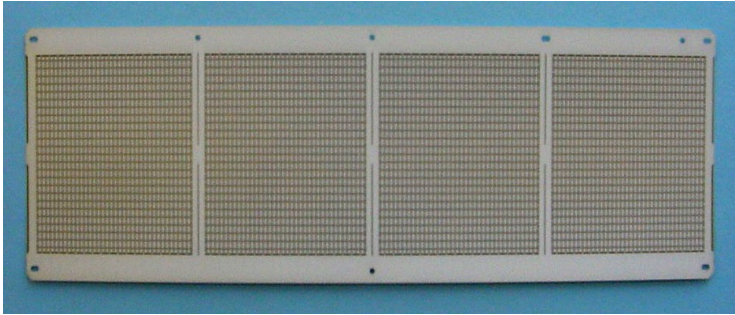
**Fig. 5. Vishay 298D M-case “leadframe less” capacitor versus competing capacitors.**

### **DEVELOPMENT OF MAP PACKAGING TECHNOLOGY FOR TANTALUM CAPACITOR**

Obviously, the manufacturing process for small-sized products requires high-precision equipment, tight tolerances, and advanced materials at each step.

#### **LEADFRAME REQUIREMENTS**

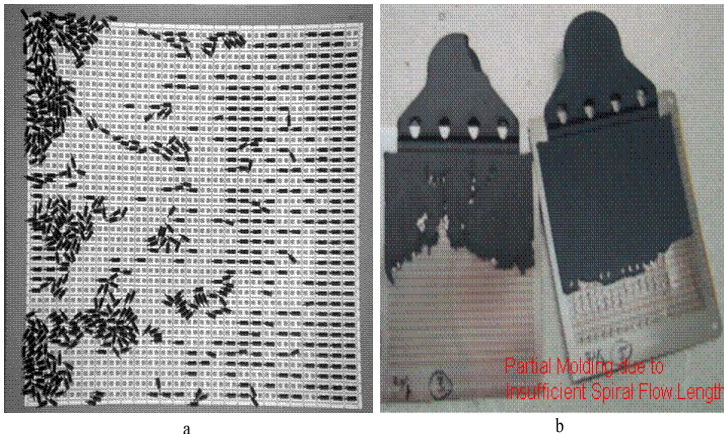
The leadframe, which serves as the base of several capacitor anode arrays, should have low thickness, rigidity and flatness (Fig. 6).



**Fig. 6. Typical MAP lead frame.**

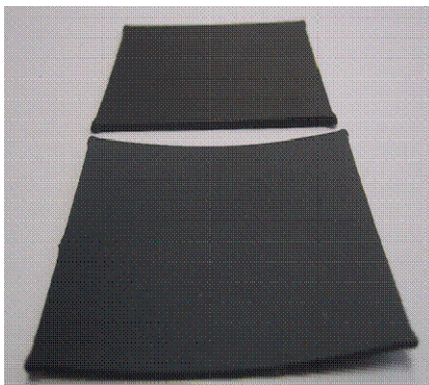
### **MOLD COMPOUND REQUIREMENTS**

Regular semiconductor-grade molding compounds were found to be inappropriate because they produce too high shear stress removing components from the leadframe. X-ray photography (Fig. 7a) illustrates capacitor anodes removed from the leadframe by the progressing encapsulant, which solidified too soon. Incomplete panel fill is another manifestation of the same problem (Fig. 7b). These phenomena usually happen when spiral flow, gel time, and viscosity of encapsulation material do not match the shape and size of the die set.



**Fig. 7 (a, b). Improper encapsulant removes anodes or causes incomplete fill.**

Another difficult issue to overcome was distortion of the molded panel. Fig. 8 shows warped molded panels due to uneven shrinkage of the encapsulating material.



**Fig. 8. Warped molded panel. Far side: straight panel molded with suitable mold compound. Near side: warped panel molded with inappropriate molding compound.**

A variety of encapsulates was analyzed in order to choose appropriate materials. MAP molding compound should meet the following criteria:

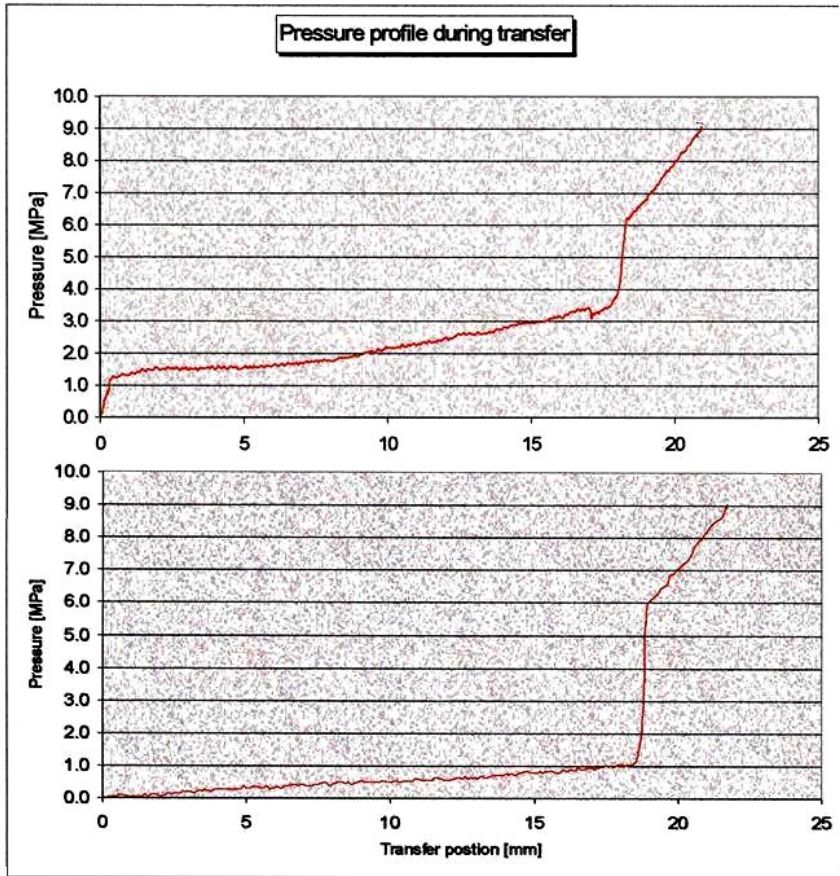
1. long spiral flow (above 55" [140mm])
2. low viscosity (max. 10 Pa.s)
3. long gel time (above 30 sec)
4. low filler cut
5. low warpage
  - low chemical shrinkage
  - low CTE1, CTE2
  - high Tg
  - high filler content

Proper combination of long spiral flow, low viscosity, and long gel time insures complete filling of the mold cavity with minimal stress induced on the product. The difference between conventional and advanced molding compound properties could be shown in the table below (Fig. 9).

<b>Parameter</b>	<b>Conventional Molding Compound</b>	<b>MAP Molding Compound</b>
Spiral Flow, 175C [cm]	50-80	140-200
Gel Time, 175C [sec]	20-40	30-50
CTE1 [ppm]	15-25	10-15
CTE2 [ppm]	45-65	40-60
Tg [C]	150-170	150-170

**Fig. 9. Mold compound parameters.**

It is clear from the graph (Fig.10) that a suitable compound creates significantly lower stress in the course of encapsulation. Low filler cut is needed to build thin and pinhole-free package walls. Low warpage (flatness) of the molded panel is important for further process steps, such as dicing.



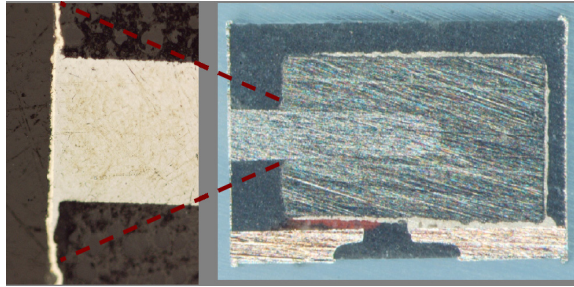
**Fig. 10. Top – Conventional molding compound: Pressure is rising during molding due to compound crystallization (short flow length and gel time).**

Bottom – Specially designed MAP molding compound: Low pressure during the molding cycle due to its long flow length and prolonged gel time.

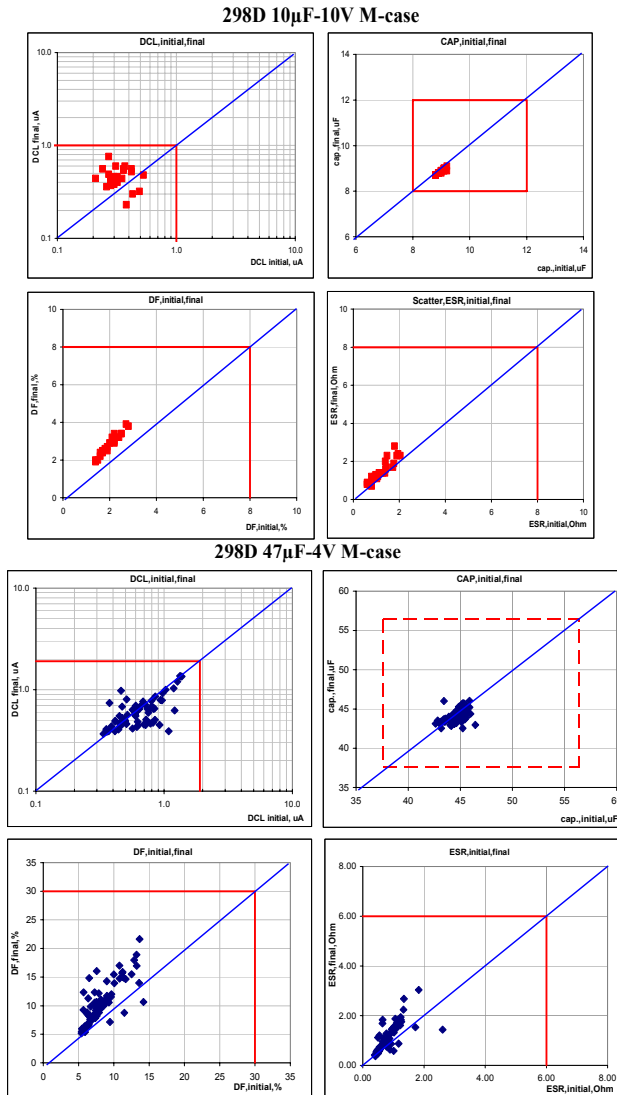
### CONSTRUCTION OF ANODE WIRE TERMINATION

As already mentioned, the most important feature of this capacitor is external connection of the tantalum wire to anode terminal, as compared to the traditional internal junction of wire and lead frame. Fig. 11 displays a cross-sectional view of the 1608, 298D Vishay capacitor. Intimate contact to outer metallization is clearly visible on the enlarged picture. Thorough investigation of this connection was performed. Multiple tests including double 260 °C Reflow, thermal shock, and other tests did not reveal any degradation of the capacitor's electrical or mechanical performance. Fig. 12 shows the excellent stability of the Vishay products, even after two consecutive cycles at 260C Lead-free Reflow profile (note; 47uF-4V presents the highest CV rating available on the market today).

As can be seen in Fig. 13, all parameters of the 10 $\mu$ F–10V M-case capacitor are well within limits through 1000 hours of 85 °C of endurance testing at full rated voltage.

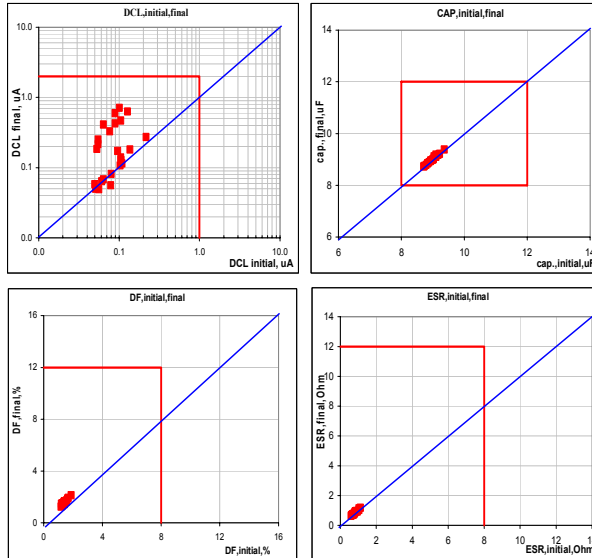


**Fig. 11. Cross-sectional view of 1608 298D Vishay capacitor.**



**Fig. 12. 298D 10 $\mu$ F-10V, 47 $\mu$ F-4V M-case capacitors: Stable electrical performance after 2 reflow cycles at 260 °C.**

### 298D 10 $\mu$ F-10V M-case

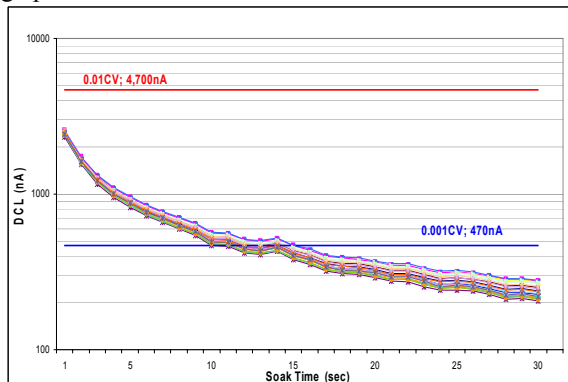


**Fig. 13. 298D 10 $\mu$ F–10V M-case capacitor: Stable electrical parameters through 2,000 hours of 85 °C of testing at full rated voltage.**

### DEVELOPMENT ROAD MAP

High volumetric efficiency of multi-array packaging (MAP) technology is suitable for development of both High Capacitance values for consumer applications and High Reliability products demanded by Military and Medical customers. As it is well known, battery operated Medical implantable devices need capacitors with extra – low DC leakage current. Extra - space available within MAP package allows utilization of Tantalum powders with specific charge half of that normally used in standard lead framed products. Lower CV powders provide much lower DC leakage current as illustrated by Fig. 14, showing performance of Vishay TM8 product.

The product range of the Vishay 298D 1608 M-case tantalum capacitor covers values from 1.0 $\mu$ F-10V to 47 $\mu$ F-4V, while the product range of TM8 products is customer demand related. In addition to advanced packaging, this twofold increase in CV/cc is achieved by usage of high charge powders and state-of-the-art tantalum anode manufacturing technology.



**Fig. 14. TM8 47 $\mu$ F–10V D-case DCL performance.**

## **CONCLUSION**

Multi-array packaging (MAP) technology provides an excellent platform for future developments of molded tantalum chip capacitors. It allows further miniaturization towards the 1005 footprint and also provides low-profile solutions in larger case sizes.

Newly developed Vishay 298D tantalum capacitors with external anode connections deliver record capacitance values in the 1608 case size. Robust design and construction of the capacitor enable reliable use in a variety of applications.

## **ACKNOWLEDGEMENTS**

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### References:

1. J. Cadwallader, "Method for Making Tantalum Chip Capacitor", US6238444B1
2. J. Cadwallader, "Tantalum chip Capacitor", US6380577B1
3. P. Vaisman, A. Eidelman, Y. Stangrit, L. Vasserman, "Surface mount capacitor and method of making the same", Patent Pending